AMENDMENTS TO THE SPECIFICATION

Amend the specification as shown below.

Amend paragraph [0016] as shown below.

[0016] Microchip 14 includes LFSR 16, MISR 18, multiplexers 38, 40, 42, 44, 46, ~~latches~~ shift registers 17, 20, 22, 24, 26, and first set of devices 28, 30, 32, 34, 36. Microchip 14 further includes LFSR 48, multiplexers 72, 74, 76, 78, 80, shift registers 52, 54, 56, 58, 60, and sets of devices 62, 64, 66, 68, 70. Microchip 14 further includes OR logic gates 82, 84, 86 and buffer driver 88. It should be noted that one or more logic devices may be in both the first set of devices 28, 30, 32, 34, 36 and the second set of devices 62, 64, 66, 68, 70.

Amend paragraph [0017] as shown below.

[0017] LFSR 16 is provided to generate a first sequence of test data that will be input into devices 28, 30, 32, 34, 36. In particular, LFSR 16 is conventional in the art and generates a pseudo-random sequence of binary values that will be transmitted through multiplexers 38, 40, 42, 44, 46 into shift registers (also called scan chains) 17, 20, 22, 24, 26. Each of the shift registers ~~18~~17, 20, 22, 24, 26 receive binary test values from LFSR 16 and then clock the values into devices 28, 30, 32, 34, 36 using a system clock signal. Each of the sets of devices 28, 30, 32, 34, 36 may comprise a plurality of combinatorial or sequential logic devices (not shown). Further, each of the sets of shift registers ~~18~~17, 20, 22, 24, 26 may receive binary output values from the combinatorial or sequential logic devices using a system capture clock signal and then shifting the binary values to an MISR 18.